Westinghouse Electric Corporation
Semiconductor Division
Youngwood, Pennsylvania 15697

Prepared by:

Ernest R. Stonebraker

CONTRACT NO. JPL-952309

DESIGN AND DEVELOPMENT OF A HIGH POWER, LOW SATURATION VOLTAGE, MULTI-CHIP SILICON SWITCHING TRANSISTOR

Mid-term Progress Report

December 1968

This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, sponsored by the National Aeronautics and Space Administration under Contract NAS7-100.

TABLE OF CONTENTS

I. INTRODUCTION

Practical experience on Contract JPL-952043 has shown that development of a single chip transistor having a saturation voltage of 0.1 volt at 75 amperes is beyond the present state-of-the-art. Two matched transistor chips operated in parallel should more closely approach 0.1 volt saturation voltage; therefore the purpose of this contract is to design and develop a dual transistor assembly to meet the above goal.

II. PROGRESS DURING THE PRESENT PERIOD

A. DESIGN CONCEPTS

At least four prime factors were considered in the design of the dual transistor assembly. They are hermeticity, electrical resistance, power dissipation, and replaceability of chips.

Reasonable solutions for each of these problems can be realized in an assembly of two flat-pack encapsulated chips. The flat-pack concept allows hermetic encapsulation of each individual chip, and assembly of matched chips. The units can be tested separately and electrically matched to insure satisfactory operation. Should one unit fail, it can be replaced without affecting the hermeticity of the other.

In order to minimize resistance conductive paths are kept short and all external contact surfaces are plated.

Power dissipation is expected to be high due to short thermal resistance paths. The two chips are in contact with the same heat sinks, thereby providing uniform heat dissipation. Emitter ballasting resistors have not been incorporated since the purpose of such resistors is to prevent "current-hogging" and subsequent burn-out of devices. In the present case, each unit is individually capable of carrying the rated current. Further, in order to insure current sharing, the units will be matched prior to assembly. Details of construction will be discussed in the following section.

B. CONSTRUCTION DETAILS

The proposed flat-pack encapsulation is shown in Figures 3 and 4. The flat pack uses the compression bond encapsulation (CBE) concept for contacting the collector, base, and emitter of the basic transistor fusion. This package differs from the stud mounted package utilized on Contracts JPL-951303 and JPL-952043 in several aspects. First, force must be applied externally to a flat pack in order to assure good contact, while a transistor fusion in the stud mounted package is compressed by internal springing. Secondly, the emitter and collector contact faces of a flat pack are identical and, therefore, interchangeable. This allows mounting of the transistors with the emitters directly in contact with a grounded heat sink if desired. Finally the narrow profile may offer advantages in electrical resistance, thermal resistance, and in lead wire inductance.

The internal details are as follows (refer to Figure 3). The encapsulation consists of an emitter seal (1) and a collector seal (2). Within the encapsulation the transistor fusion (8) is seated on the silver membrane of the collector seal. The silver membrane is ductile and conforms to the collector side of the transistor fusion. In the stud mounted package, an additional silver foil must be included for this purpose. Contact to the emitter and base regions of the transistor fusion is made with a silver-Teflon emitter-base contact assembly (7). The base lead (6) is insulated and passes through a pressure contact (5) and makes contact to the weld flange (3) of the emitter seal. The pressure on the emitter portion of the silver-Teflon contact assembly completes the contact through the silver membrane of the emitter seal to the emitter contact pad (4). The assembly of two parallel devices is shown in Figure 4. The heat sink (9) is manufactured by Astrodyne, Inc., and is their extrusion Type 2506. This heat sink is designed for natural convection and was chosen because of its large surface area and low thermal resistance.

It should be noted that the remainder of the assembly parts can be used on any flat surface. The heat sink is included to facilitate testing and rating.

The top portion of the assembly consists of a collector contact bar (5). This bar serves several purposes. The first is that it provides a low resistance electrical contact to the collector of the flat packages. Since the thermal conductivity of the copper is about twice that of the aluminum heat sink, it will serve to dissipate the heat from the devices to the heat sink much faster and over a much larger area than if the devices were mounted directly on the heat sink. The flat packages (1) are located on the collector contact bar (5), and an emitter contact bar (2) is located on the emitter contact area of the flat package. The top compression bar (4) is located and held in position over the emitter contact bar by two dowel pins (3). The dowel pins fit in a milled groove on both the emitter and top bars. The dowel pins also prevent misalignment of the flat package due to thickness variations and will serve to apply the required force to the center of the flat packages. Alignment of the assembly is accomplished by the compression bolt (15) and insulator (13). The bolt along with the compression nut (16) and Belleville springs (14) maintain the required force on the flat package. In order to provide additional support to the heat sink, a support plate (1) is located next to the heat sink. Insulation of the emitter from the collector is accomplished by the insulator (13) and mica washers (11). A compression washer (12) provides protection for the mica from the Belleville springs. The compression nut is specially designed to provide alignment for the Belleville springs.

The proposed force required to provide low thermal and electrical resistance is about 2000 lb. This will mean that each flat package will be supporting about 1000 lb., which from past experience with stacks and flat package assemblies, should be adequate.

C. ASSEMBLY TECHNIQUES AND PROBLEMS

After assembling the parts by hand, the entire assembly is placed in a laboratory press and compressed with a force of 2000 lb. The nut is now tightened, maintaining the desired force.

On the first flat pack encapsulated devices, emitter-base shorts developed when the units were compressed. These shorts are probably due to a slight misalignment of the silver-Teflon contact assembly. The same problem is frequently encountered in the compression bonded stud mount package, but that package can be disassembled and the contact assembly realigned. The flat pack must be welded immediately after assembly, thus realignment of the emitter contact is not possible. The inside diameter of the foil on the emitter contact will be increased to provide greater tolerance to misalignment.

In addition to changing dimensions, a new approach is being tried; that is, the use of a silver plated Teflon contact. By using this type of contact the following advantages are expected:

1. More accurate contact area dimensions will be achieved.
2. Cleaner contacts by avoiding contamination that has been present with folded contacts.
3. Alignment will be improved due to less flow of Teflon cushion.

III. PROGRAM FOR NEXT PERIOD

A. The new silver-Teflon contacts will be evaluated.

B. Transistors will be fabricated using the epitaxial base process developed on JPL-952043.

C. Measurements will be made to determine the effect of parallel operation of both matched and purposely mismatched transistors.

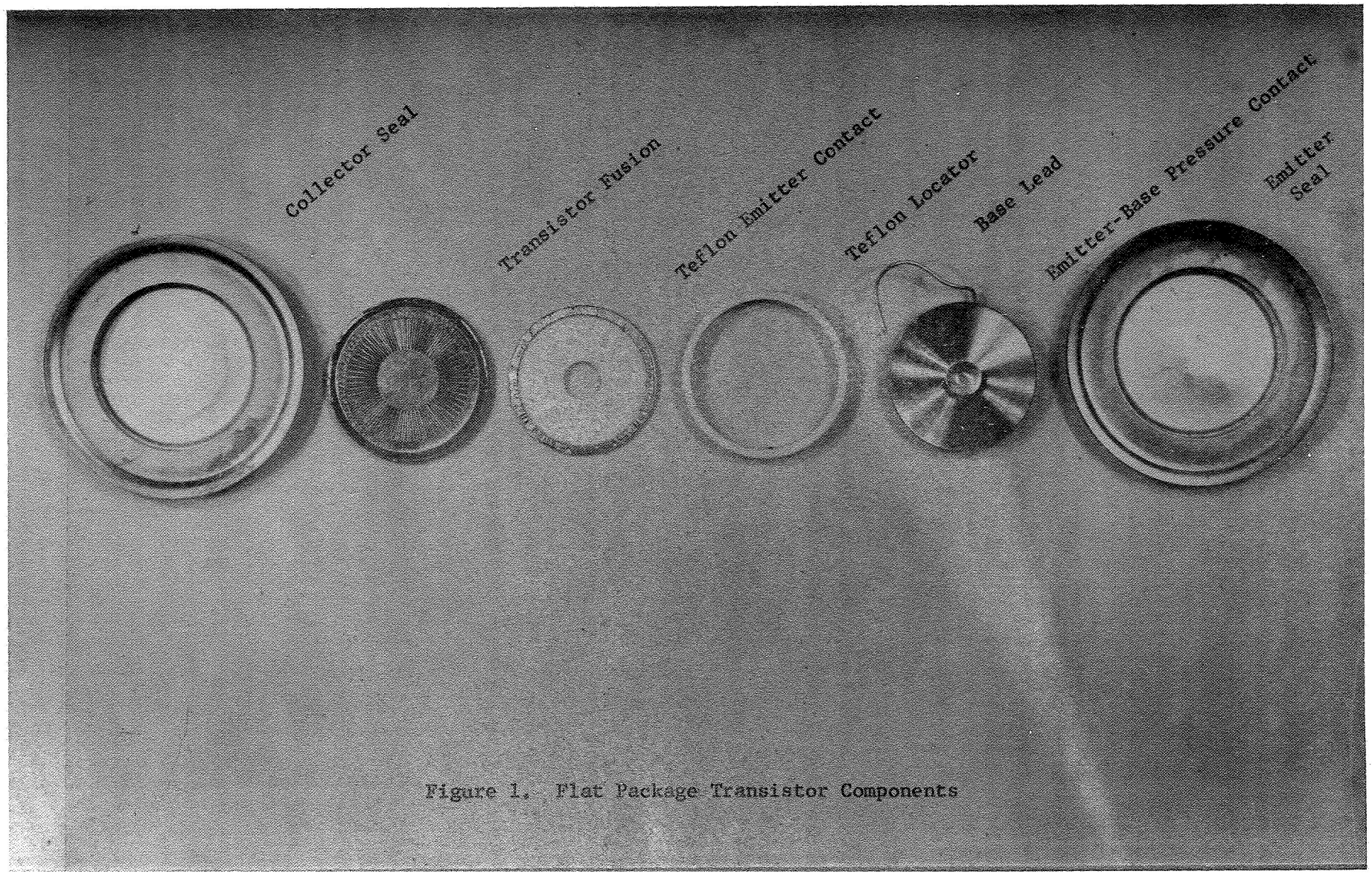


Figure 1. Flat Package Transistor Components

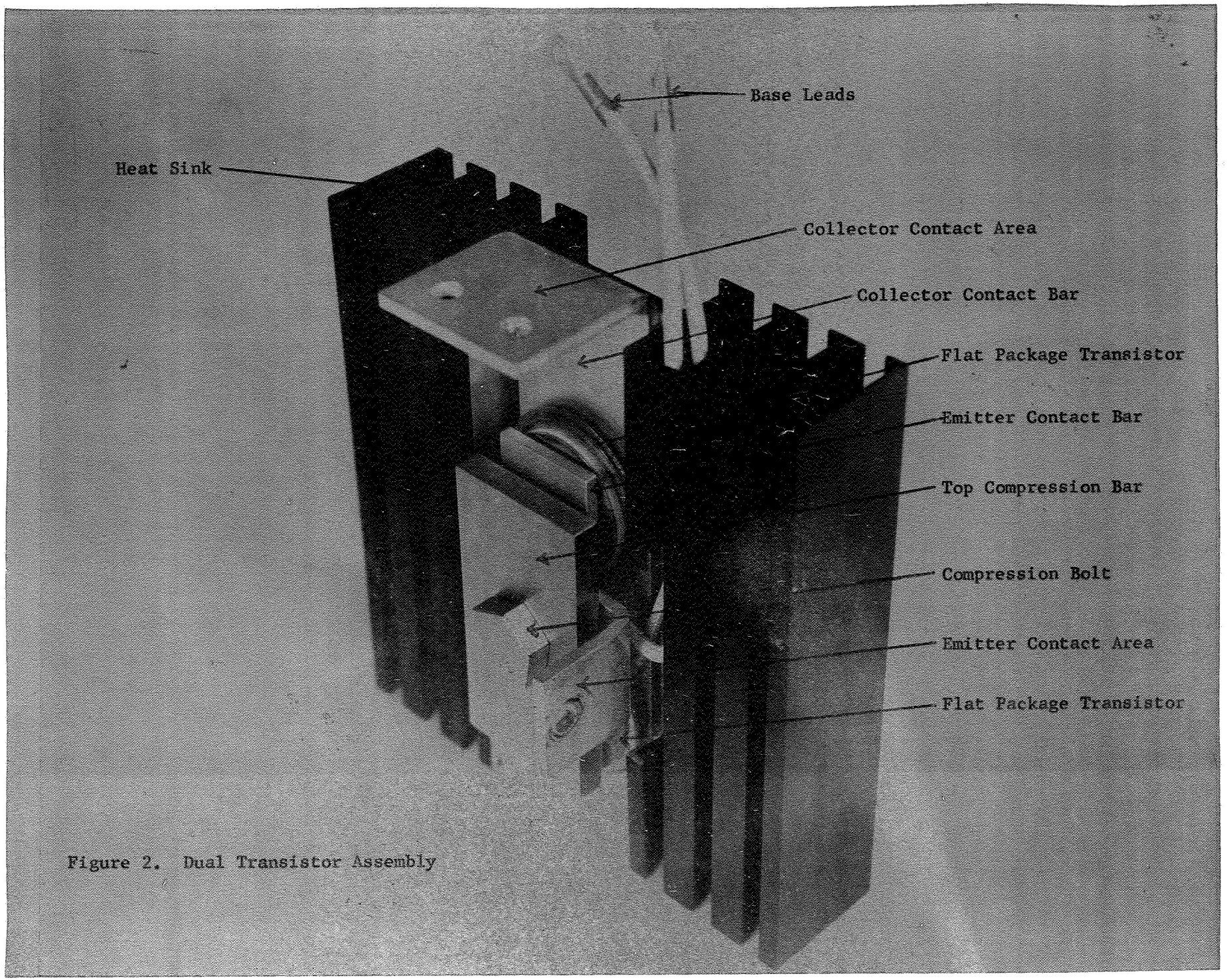
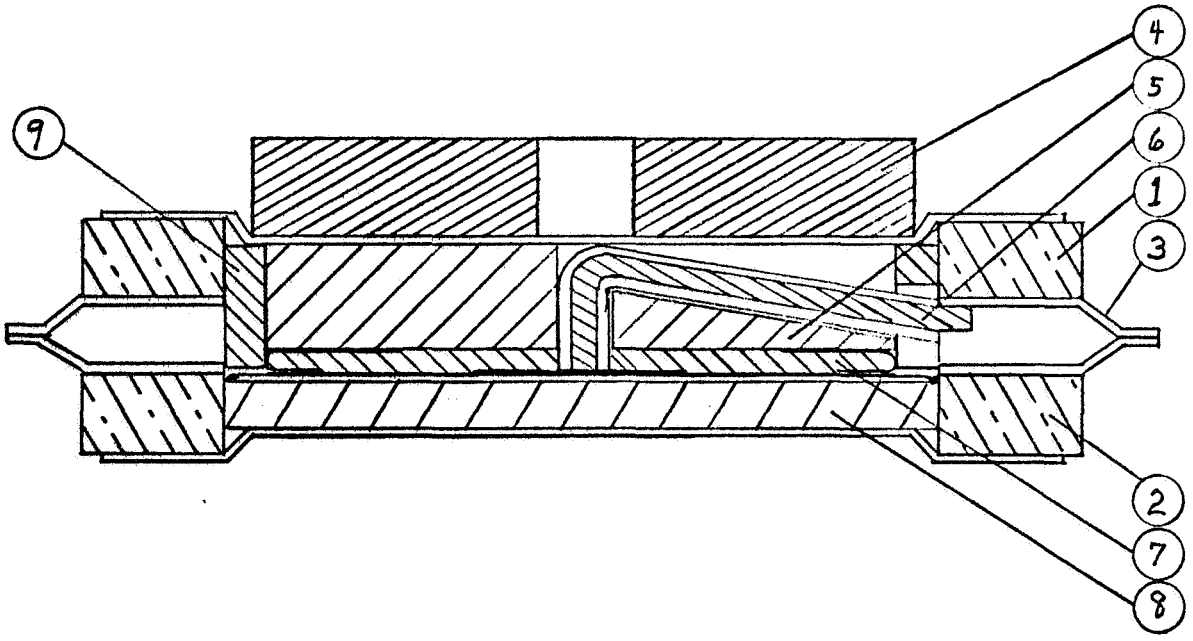


Figure 2. Dual Transistor Assembly

WESTINGHOUSE ELECTRIC CORPORATION

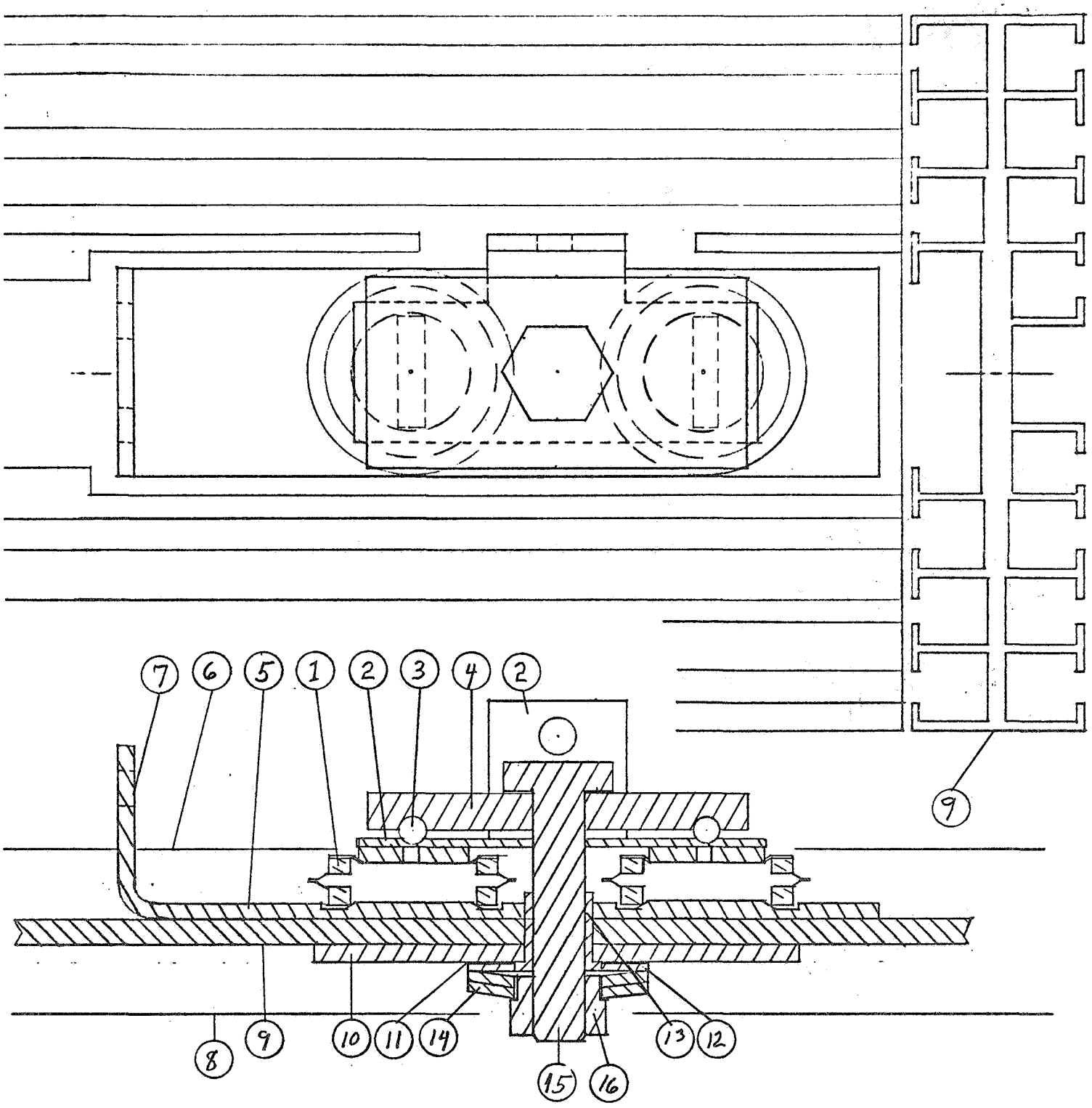
FLAT PACKAGE 1401 TRANSISTOR



(1) Emitter Seal
(2) Collector Seal
(3) Weld Flange
(4) Emitter Contact Pad
(5) Emitter Base Pressure Contact
(6) Base Lead
(7) Teflon Emitter Base Contact
(8) Transistor Fusion
(9) Teflon Locator

FIGURE 3

EDSK-A-335615



(1) Flat Package 1401
(2) Emitter Contact Bar
(3) Dowel Pin Aligner
(4) Top Compression Bar
(5) Collector Contact Bar
(6) Top Fin Limit
(7) Collector Contact Area
(8) Bottom Fin Limit
(9) Heat Sink
(10) Support Plate
(11) Mica Insulation
(12) Compression Washer
(13) Insulator
(14) Belleville Springs
(15) Compression Bolt
(16) Compression Nut

FIGURE 4

JPL 952309 Assembly
EDSK-A-335616